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EXAMINER	
DANG, TRUNG Q	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,553	DE FRESART ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 34-69 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 34-69 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/22/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 34, 36, 38, 39, 42, 55, 57, 65, 67, and 68 are rejected under 35 U.S.C. 102(b) as being anticipated by Malhi (U.S. Pat. 5,696,010 cited by applicants).

With reference to the figure drawing 4, Malhi teaches a method of manufacturing a semiconductor component comprising the steps of:

providing a substrate (12) having a surface ;

forming by a non LOCal Oxidation of Silicon (LOCOS) process a non-electrically conductive region (55) substantially located below a substantially planar plane defined by the surface of the substrate;

forming a drift region (14) in the substrate;

forming a channel region (23) in the substrate, at least a portion of the drift region located between the channel region and the non-electrically conductive region; and forming an electrically floating region (21) in the substrate and contiguous with the non-electrically conductive region.

The following interpretation explains as to why the Malhi's reference reads on limitations of independent claim 34:

- The non-electrically conductive region (isolation region (55)) formed by a trench process, which is a non-LOCOS process.

- The upper portion of the drift region (14) located between the channel region (23) and the non-electrically conductive region (25).

- Isolation region (21) is considered as an electrically floating region because it electrically isolates channel region (23) from substrate (12), i.e., isolation region (21) floats over the substrate (12).

- The electrically floating region (21) is contiguous (i.e., in close proximity without actually touching) with the non-electrically conductive region (25).

- As for claim 57, Fig. 4 shows the drift region (14) is located at least partially under the gate electrode (26).

3. Claims 34, 44-54, 56, 61, 62, and 64 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (U.S. Pat. 6,087,232).

With reference to the figure drawings 2a, 2b, 2d, and 2f, Kim et al. teach a method of manufacturing a semiconductor component comprising the steps of:

providing a substrate comprises p-type layers (20), (21) and an n-type layer (22) (Fig. 2a and related text) having a surface;

forming by a non LOCal Oxidation of Silicon (LOCOS) process a non-electrically conductive region (26) (Figs. 2e-2f) substantially located below a substantially planar plane defined by the surface of the substrate;

forming a drift region (22) in the substrate;

forming a channel region (layer (21) where a channel is formed therein) in the substrate, at least a portion of the drift region (22) located between the channel region (21) and the non-electrically conductive region (26); and

forming an electrically floating region (25) in the substrate and contiguous with the non-electrically conductive region (26).

The following interpretation explains as to why the Kim's reference reads on the claimed limitations:

For claim 34, Fig. 2a shows the substrate comprises layers (20), (21), and (22) having an original surface. Fig. 2b shows field oxide 23B (FOX) penetrates below the original surface of the substrate. Figs. 2d-2e show the FOX has been removed

exposing a new surface that is below the original surface of the substrate. Figs. 2e-2f show the deposition of a TEOS oxide layer and an etch process to form a TEOS non-electrically conductive region (26) (middle TEOS portion in Fig. 2f) on the new surface of the substrate. Since the new surface is below the original surface, at least a portion of the TEOS non-electrically conductive region (26) is located below a substantially planar plane defined by the surface of the substrate. The non-electrically conductive region (26) is formed by deposition, which is a non-LOCOS process. Furthermore, p-type region (25) is considered as an electrically floating region because it helps the drift region (22) to be easily depleted, and when the drift region (22) is fully depleted p-type region (25) is electrically floated above channel region (21).

As for claim 51, see region 29 for the claimed drain region.

As for claim 53, Fig. 2f shows at least a portion of the electrically floating region (25) is located between the non-electrically conductive region (26) and the channel region (21) and at least a portion of the electrically floating region (25) is located underneath the non-electrically conductive region (26).

As for claim 56, since the channel region (21) has the same conductivity type with that of the substrate (20), the channel region (21) is electrically coupled to the substrate (20).

As for claim 62, the top portion (corresponds to the claimed first portion) of the electrically floating region (25) is located at least partially underneath the non-

electrically conductive region (26), and the bottom portion (corresponds to the claimed second portion) of the electrically floating region (25) is located between a portion of the drift region (22) and a portion of the non-electrically conductive region (26).

As for claim 64, see the gate dielectric 27.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 37, 40, 43, 66, and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malhi as above in view of Yasuhara et al. (U.S. Pat. 6,353,252).

Malhi teaches a method of manufacturing a semiconductor component as noted in the above 102(b) rejection.

As for claims 37, 40, 66, Malhi differs from the claims in that while Malhi fills the trench with oxide, the claims call for a semi-insulative material as a trench filler together with a thermal oxide trench liner.

Yasuhara et al. teach a method comprising a formation of an isolation trench in which a thermal oxide layer 13 is formed along the trench walls prior to filling

the trench with a semi-insulating polycrystalline silicon (SIPOS) film 14 (Fig. 2 and col. 5, lines 8-12).

The subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to fill the isolation trench of Malhi in the manner as suggested by Yasuhara et al. because such trench fill materials are known in the art for the isolation purpose, and the substitution of a known material to achieve the same goal would have been within the level of one skilled in the art, absent a showing of criticality by applicants.

As for claims 43 and 69, Yasuhara et al. in col. 5, lines 28-29 suggest that "The resistance of the film 14 can be adjusted by the concentration of oxygen contained therein..." Thus, one skilled in the art would recognize that incorporating oxygen into the SIPOS film 14 would increase the resistance of the film because oxygen atoms would react with silicon atoms in the SIPOS to form silicon oxide that possesses insulation property. It would have been obvious to one having ordinary skill in the art to incorporate oxygen into SIPOS film 14 because this would increase the resistance of the SIPOS film 14, hence increasing the isolation property of the trench. Moreover, introducing oxygen atoms into a region by implantation is well known in the art. Thus, the limitation regarding implanting a dose of oxygen into the surface of the substrate at location corresponding to non-electrically conductive region (i.e., trench isolation region) is meet.

5. Claims 34-40, 42, 45, 48-50, 55, and 57-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tung (U.S. Pat. 6,110,803 cited by applicants) in view of Kitamura et al. (U.S. Pat. 5,844,275).

With reference to the figure drawing 2F, Tung teaches a method of manufacturing a semiconductor component comprising the steps of:

providing a p-type substrate (200) having a surface;

forming by a LOCal Oxidation of Silicon (LOCOS) process a non-electrically conductive region (228) substantially located below a substantially planar plane defined by the surface of the substrate;

forming a drift region (250) in the substrate;

forming a channel region (221) in the substrate, at least a portion of the drift region (250) located between the channel region (221) and the non-electrically conductive region (228); and forming an electrically floating regions (219) in the substrate and contiguous with the non-electrically conductive region.

Note that p-type regions (219) are electrically floating regions because they help the drift region (250) to be easily depleted, and when the drift region (250) is fully depleted p-type regions (219) are electrically floated above the substrate (250).

Tung differs from the claims in that while Tung forms the non-electrically conductive region (228) by LOCOS process, the claims call for a non-LOCOS process to form the same.

Kitamura et al. teach an advantage of a trench isolation over the conventional LOCOS isolation (Figs. 3A-3B and col. 6, lines 1-6; col. 9, lines 10-16; col. 10, lines 3-18).

It would have been obvious to one of ordinary skill in the art to modify Tung's process by forming the non-electrically conductive region (228) by a trench isolation process as suggested by Kitamura et al. because of the advantages mentioned in the above sections namely the withstand voltage is improved, the on-resistance and the cell pitch are reduced, thereby improving the performance of the device and increasing chip density per wafer.

For claim 35, see Figs. 2A and 2B for the formation of the channel region (221) and the electrically floating regions (219) occurs simultaneously with each other.

For claims 37-39, 66-68, see col. 5, line14 and col. 8, lines 21-22 for the materials of the trench fillers.

As for claim 40, the Examiner takes official notice that lining the trench walls with a thermal oxide layer before filling the trench with semi-insulating polysilicon is an old practice in the art.

For claim 42, Figs. 6 and 7 show planar trench surfaces, i.e., the trench fill materials are planarized.

For claim 55, channel region (221) is electrically isolated from the substrate (250) located underneath the channel region because the channel region and the substrate have opposite type of conductivity.

For claims 62 and 63, when all three p-type regions (219) are considered as a single electrically floating region, the electrically floating region comprises a first portion (e.g., the first p-type region (219)) and the second portion (e.g., the second p-type region (219)), and the first portion is separate from the second portion as shown in Fig. 2F.

6. Claims 43 and 69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tung taken with Kitamura et al. as applied to claims 34-40, 42, 45, 48-50, 55, and 57-68 above, and further in view of Yasuhara et al. cited above.

The combination of Tung and Kitamura et al. teaches a process as mentioned above. The combined process differs from the claims in not disclosing the claimed step of implanting a dose of oxygen into the surface of the substrate at location corresponding to the non-electrically conductive region. However, Yasuhara et al. in col. 5, lines 28-29 suggest that "The resistance of the film 14 can be adjusted by the concentration of oxygen contained therein..." Thus, one skilled in the art would recognize that incorporating oxygen into the SIPOS film would increase the resistance of the film because oxygen atoms would react with silicon atoms in the SIPOS to form silicon oxide that possesses insulation property. Therefore, in the

case where the trench is filled with a semi-insulating polysilicon (SIPOS) as taught in Kitamura, it would have been obvious to one having ordinary skill in the art to incorporate oxygen into SIPOS film because this would increase the resistance of the SIPOS film, hence increasing the isolation property of the trench. Moreover, introducing oxygen atoms into a region by implantation is well known in the art. Thus, the limitation regarding implanting a dose of oxygen into the surface of the substrate at location corresponding to non-electrically conductive region (i.e., trench isolation region) is meet.

7. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tung taken with Kitamura et al. as applied to claims 34-40, 42, 45, 48-50, 55, and 57-68 above, and further in view of Ishikawa (U.S. Pat. 6,277,706).

The combination of Tung and Kitamura et al. teaches a process as mentioned above. The combined process differs from the claims in not disclosing the claimed limitation of densifying the trench fill material. However, Ishikawa teaches that densifying an oxide filled in the trench would eliminate pits, which would have caused by subsequent planarizing process (col. 5, lines 14-19, lines 32-40). Thus, in the case where the trench is filled with an oxide as taught in Kitamura, it would have been obvious to one having ordinary skill in the art to densify the filled oxide as suggested by Ishikawa because this would eliminate pits hence improves reliability of the device.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

08/20/04